

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S3	0	("4080650" "5321828" "5367550" "5754839" "5774724" "6154857" "6182208" "6751751" "6795964").PN.).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/07 15:19
S2	0	("4080650" "5321828" "5367550" "5754839" "5774724" "6154857" "6182208" "6751751" "6795964").PN.).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/10/07 15:19
S5	135	count with breakpoint	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/10/07 15:40
S6	34	count with breakpoint with number	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/10/07 15:41
S7	4	S4 and S5	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/10/07 15:55
S4	9	("4080650" "5321828" "5367550" "5754839" "5774724" "6154857" "6182208" "6751751" "6795964").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/10/07 15:55
S8	42	gprof	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/10 07:15
S1	0	("4080650" "5321828" "5367550" "5754839" "5774724" "6154857" "6182208" "6751751" "6795964").PN.).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/10/10 07:15
L2	97	count\$3 with number with breakpoint	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/10/10 08:22
L1	9	("4080650" "5321828" "5367550" "5754839" "5774724" "6154857" "6182208" "6751751" "6795964").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/10/10 08:22


[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

 Search: ☒ The ACM Digital Library ☐ The Guide

gprof

SEARCH


[Feedback](#) [Report a problem](#) [Satisfaction survey](#)
Term used **gprof**

Found 193 of 164,603

Sort results by

relevance

[Save results to a Binder](#)Try an [Advanced Search](#)Try this search in [The ACM Guide](#)

Display results

expanded form

[Search Tips](#)
☐ Open results in a new window

Results 1 - 20 of 193

Result page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [next](#)Relevance scale ☐ ☐ ☐ ☐ ☐1 [Gprof: A call graph execution profiler](#)

Susan L. Graham, Peter B. Kessler, Marshall K. McKusick

June 1982 **ACM SIGPLAN Notices , Proceedings of the 1982 SIGPLAN symposium on Compiler construction**, Volume 17 Issue 6Full text available: [pdf\(684.69 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Large complex programs are composed of many small routines that implement abstractions for the routines that call them. To be useful, an execution profiler must attribute execution time in a way that is significant for the logical structure of a program as well as for its textual decomposition. This data must then be displayed to the user in a convenient and informative way. The gprof profiler accounts for the running time of called routines in the running time of the routines ...

2 [1982: gprof: a call graph execution profiler](#)

Susan L. Graham, Peter B. Kessler, Marshall K. McKusick

April 2004 **ACM SIGPLAN Notices**, Volume 39 Issue 4Full text available: [pdf\(1.48 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#)

We extended the UNIX® system's profiler by gathering arcs in the call graph of a program. Here is it 20 years later and this profiler is still in daily use. Why is that? It's not because there aren't well-known areas for improvement. Large complex programs are composed of many small routines that implement abstractions for the routines that call them. To be useful, an execution profiler must attribute execution time in a way that is significant for the logical structure of a program as well a ...

3 [Reconfigurable computing: architectures and applications: Using reconfigurability to achieve real-time profiling for hardware/software codesign](#)

Lesley Shannon, Paul Chow

February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**Full text available: [pdf\(228.02 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Embedded systems combine a processor with dedicated logic to meet design specifications at a reasonable cost. The attempt to amalgamate two distinct design environments introduces many problems, one being how to partition a single design for the two platforms to achieve the best performance with the least effort. Since the latest FPGA technology allows the integration of soft or hard CPU cores with dedicated logic on a single chip, this presents new opportunities for addressing hardware/software ...